REMARKS

Applicants have cancelled one independent and one dependent claim and introduced one new independent claim and one new dependent claim in the same species as the cancelled claims.

Applicants submit this Amendment "E" and Response for the Examiner's consideration. Reexamination and reconsideration of the application, in view of the following remarks are respectfully requested.

1. STATUS OF THE CLAIMS

Claims 1-33 and 45-46 were presented for examination and they stand rejected under 35 U.S.C. § 103(a). These rejections are addressed below.

2. RESPONSE TO REJECTIONS

2.1. *Claim Rejections Under 35 U.S.C. § 103(a)*

Claims 1-33 and 45-46 stand rejected under 35 U.S.C. § 103(a) either in view of the combination of Japanese Patent 62-48028 (hereinafter "JP'028") and Wolf, vol. 1, pp. 323-24 (hereinafter "Wolf') or in view of this combination together with Japanese Patent 63-300526 (hereinafter "JP'526"). English translations of JP'028 and JP'526 are part of the record, and thus cites to and quotes from these patents are given below without providing additional copies of these translations.

Applicants respectfully submit that the pending claims patentably distinguish over the cited references even if these references were combinable. Distinguishing features between the pending claims and the teachings provided in the cited patents include the following:

(a) Both JP'028 and JP'526 form silicon oxide predominantly at the center of the field region.

JP'028 forms silicon oxide predominantly at the center of the field region by selectively forming an implant defect area at the center of the field region which will in a successive operation form "oxide film 7 with only its central area 7a thickened." Translation JP'028, p. 4, last paragraph, *ll.* 6-7; Figs. 1c-1d and legend for feature 7a therein. Si ion implantation according to JP'028 is performed through an opening that is narrower than the opening through which oxidation is performed. *See.* Translation JP'028, Figs. 1(b)-(c), and corresponding legends.

According to JP'526, impurity implantation is performed throughout an opening that is wider than the opening through which thermoxidation is performed. Therefore, silicon dioxide film will be significantly thicker at the center of the opening and will become thinner under the spacers, which are the elements that reduce the wider opening through which impurity implantation is peformed to the narrower opening through which thermal oxidation is performed. *See,* Translation JP'526, Figs. 1(b), 1(d), 1(f), and corresponding legends.

In contrast, the pending claims recite, explicitly or by incorporation from the corresponding independent claims, operations such as ion implantation and oxidation that are performed through the same opening and opening width.

(b) Both JP'028 and JP'526 rely on the formation of at least one layer within the field region that modifies the width of the opening through which impurity (JP'526) or ion (JP'028) implantation takes place on the one hand, and through which exposure to oxidant takes place on the other hand. These layers are exemplified by second oxide-proof film 6 in JP'526 (*see, e.g.*, Translation JP'526, Fig.1(c) and corresponding legends), and by photoresist implanting mask 4 in JP'028 (*see, e.g.*, Translation JP'028, Fig.1(b) and corresponding legends). In contrast, the pending claims recite that

no layer within the field region is formed such that it would enlarge or reduce the exposure area of the substrate to the different agents, such as implantation ions and oxidant.

(c) The field oxides formed according to JP'028 encroach under nitride film mask 3a to an extent such that they even distort such nitride film mask, as shown therein in Fig. 1(c). The field oxides formed according to JP'526 extend below and beyond nitride spacers 9. The methods in the pending claims recite operations that lead to field oxides with reduced bird's beak structures with minimal encroachment under, for example, the nitride mask, and with substantially no bird's beak structure under the spacers recited therein.

(d) The cited references do not teach positively recited operational criteria for method steps such as implantation ion selection and oxidation kinetics of oxide formation.

(e) The cited references do not teach the reduced and positively recited smaller number of operations for ion implantation and oxidation.

(f) Wolf does not provide any teaching to overcome these differences between the presently claimed methods and the methods disclsoed in JP'028 and/or JP'526.

(g) In addition to distinguishing features such as those set forth in previously filed Amendments, distinguishing features of the presently claimed methods such as those indicated herein lead to methods to form oxide regions with increased miniaturization, increased insulation efficacy, and with fewer operations. The importance and the desirability of advantages such as these, and the failure of conventional techniques, including photolithography concerning the width of embodiments of the unmasked opening as recited in some of the pending claims, to provide such features are set forth in the present Application as originally filed.

Applicants incorporate herein the reasoning, cites and quotes set forth with respect to the cited art in Amendment "D" and Response filed June 13, 2001.

For reasons such as those set forth above, even if the cited references were combinable, it is respectfully submitted that they may not establish a *prima facie* case of obviousness with respect to the present claims.

Consequently, Applicants respectfully request the reconsideration and withdrawal of this rejection.

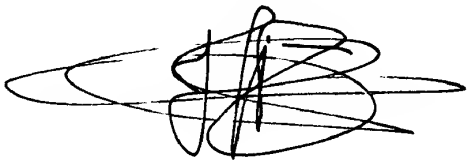
3. CONCLUSIONS

In view of the above, Applicants respectfully maintain that the present Application is in condition for allowance. Reconsideration of the rejections is requested. Allowance of the pending claims at an early date is solicited.

In the event that the Examiner finds any remaining impediment to a prompt allowance of this application which could be clarified by a telephonic interview, or which is susceptible to being overcome by means of an Examiner's Amendment, the Examiner is respectfully requested to initiate the same with the undersigned attorney.

Dated this 26th day of November 2001.

Respectfully submitted,



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Marked up Version of the Pending Claims Under 37 C.F.R. § 1.121(c)(1)(ii):

Please amend the following claims in accordance with 37 C.F.R. § 1.121(c)(1)(ii), by which Applicants submit the following marked up version only for claims being changed by the current amendment, wherein the markings are shown by brackets (for deleted matter) and/or underlining (for added matter):

2. (Thrice Amended) A method as recited in Claim [1] 47, wherein said implantation ions comprise ions of said first material and ions that are [ions] different from said ions of said first material[are bombarded concurrently with said ions of said first material into said exposed region of said volume of semiconductor material].

3. (Twice Amended) A method as recited in Claim 2, wherein the [implanted] implantation ions of said first material comprise silicon ions.

4. (Twice Amended) A method as recited in Claim 3, wherein said first material [is composed of] comprises monocrystalline silicon.

6. (Thrice Amended) A method as recited in Claim [5] 47, further comprising forming [a] spacers in said masking substrate, wherein said unmasked opening is comprised between two adjacent spacers, and each of said spacers extends from the substrate assembly to the top of and in contact with said masking substrate [around the opening of the hard mask, said spacer extending from the volume of semiconductor material composed of the first material to make contact with the hard mask, wherein said bombarding an exposed region of a volume of semiconductor material composed of a first material with ions of said first material implants said ions of said first material immediately adjacent to but not through the spacer around the opening in the hard mask].

7. (Twice Amended) A method as recited in Claim 6, wherein said forming [a] spacers [around the opening of the hard mask] further comprises:

depositing a layer of spacer material over the opening in the [hard mask] masking substrate; and

etching the layer of spacer material [over the opening in the hard mask] to form the spacers around the unmasked opening[in the hard mask].

9. (Thrice Amended) A method as recited in Claim 7, wherein said etching the layer of spacer material is an anisotropic etch[, and wherein the spacer is one of a pair of spacers through which the ions of said first material are implanted between but not through the pair of spacers around the opening in the hard mask and into the exposed region, wherein the exposed region is situated between the pair of spacers].

10. (Thrice Amended) A method as recited in Claim 9, wherein said opening width is [the pair of spacers are separated by a distance] in the range from about 0.05 micrometers to about 0.1 micrometers.

11. (Thrice Amended) A method as recited in Claim [1] 47, further comprising the steps, prior to said bombarding through said unmasked opening [an exposed region of a volume of semiconductor material composed of a first material with ions of said first material,]of:

forming a pad oxide layer [over the volume of] on said first semiconductor material [composed of the first material];

forming a masking substrate comprising a nitride layer over the pad oxide layer;

forming a photoresist mask over the nitride layer; and

selectively removing the nitride layer through the photoresist mask to expose [an] through said unmasked opening [to the volume of] said first semiconductor material [composed of the first material at the region], wherein the first semiconductor material is oxidized in the region within said unmasked [the] opening[to the volume of semiconductor material composed of the first material].

12. (Thrice Amended) A method as recited in Claim 11, wherein the photoresist mask is removed after said bombarding through said unmasked opening of said first [an exposed region of a volume of] semiconductor material [composed of a first material] with implantation ions of said first material.

14. (Thrice Amended) A method as recited in Claim [1] 47, wherein said semiconductor material has a top surface, and wherein said implantation ions are directed towards said first semiconductor material [the exposed region of a volume of semiconductor material has a top surface, and the ions of said first material are implanted into the exposed region] in a direction that is within ten degrees from a direction that is orthogonal to the top surface.

15. (Thrice Amended) A method as recited in Claim [1] 47, wherein said forming an oxide [oxidizing said first material in said exposed region] further comprises heating [the] said substrate assembly while exposing the substrate assembly to oxygen.

16. (Thrice Amended) A method as recited in Claim [1] 47, wherein said first [the volume of] semiconductor material [composed of said first material] comprises a monocrystalline material having a lattice structure, wherein the [implanted] implantation ions [of said first material in the monocrystalline material] cause the lattice structure of the monocrystalline material to become partially randomized at the region into which [the] said ions [of said first material] are implanted.

17. (Twice Amended) A method as recited in Claim 16, wherein both the monocrystalline material and [the] said implantation ions [of said first material] comprise silicon.

18. (Thrice Amended) A method as recited in Claim [1] 47, wherein said [oxidizing] exposing said implanted region [first material in said exposed region] is conducted at a pressure in the range [of] from about 1 atmosphere to about 25 atmospheres.

19. (Thrice Amended) A method as recited in Claim [1] 47, wherein [oxidizing] said exposing said implanted region [said first material in said exposed region] is conducted at a pressure in the range [of] from about 5 atmospheres to about 25 atmospheres.

20. (Thrice Amended) A method for forming an oxide region on a substrate assembly, the method comprising the steps of:

forming a hard mask over a volume of silicon of a substrate assembly;

forming an opening in the hard mask to expose a region of the volume of silicon;

bombarding the exposed region of the volume of silicon with silicon ions through the opening in the hard mask so as to leave unaltered the conductivity type of the exposed region of the volume of silicon; and

oxidizing the volume of silicon by exposure through said opening to oxygen of an exposed surface thereof to form silicon dioxide substantially only at the region [by exposure of the] exposed [region] to oxygen, wherein said silicon dioxide has substantially uniform thickness throughout said region, wherein said bombarding and said oxidizing are performed through said opening having a width that is substantially the same at said bombarding as it is at said oxidizing, and wherein no additional layer is formed within said opening after said bombarding and prior to said oxidizing.

21. (Thrice Amended) A method as recited in Claim 20, further comprising forming a spacer around the opening in the hard mask, said spacer extending from the volume of silicon to contact the hard mask, wherein said bombarding the exposed region of the volume of silicon with silicon ions through the opening in the hard mask implants ions immediately adjacent to but not through the spacer around the opening in the hard mask, and wherein said oxidizing and said bombarding are performed through the same opening.

22. (Twice Amended) A method as recited in Claim 21, wherein said forming a spacer around the opening in the hard mask comprises:

depositing a layer of spacer material over the opening in the hard mask; and

anisotropically etching the layer of spacer material at the opening in the hard mask to form the spacer situated around the opening of the hard mask.

32. (Thrice Amended) A method for forming an oxide region on a substrate assembly, the method comprising the steps of:

forming a hard mask over a pad oxide layer situated on a volume of silicon of a substrate assembly, the substrate assembly having a top surface;

forming an opening in the hard mask to expose a region of the volume of silicon, said region of said volume of silicon compris[es]ing monocrystalline silicon having a lattice structure;

depositing a layer of silicon nitride over the opening of the hard mask;

etching the layer of silicon nitride and the pad oxide layer to form a pair of silicon nitride spacers situated on opposite sides of the opening of the hard mask and having said exposed region of the volume of silicon therebetween, each said silicon nitride spacer extending from the volume of silicon to contact the hard mask; and

forming silicon dioxide in the region between said pair of spacers by kinetically regulating silicon oxidation, wherein said kinetically regulating silicon oxidation comprises:

implanting silicon ions between but not through the pair of silicon nitride spacers and through the opening in the hard mask into the exposed region of the volume of silicon such that the direction that the silicon ions are implanted into the exposed region is within ten degrees of a direction that is orthogonal to the top surface of the substrate assembly, wherein the implanted silicon ions do not substantially alter the conductivity type of the region, and wherein the implanted silicon ions in the monocrystalline silicon in the exposed region cause the lattice structure thereof to become partially randomized; and

heating the substrate assembly [while] and exposing the substrate assembly to oxygen so as to form silicon dioxide at the exposed region, whereby the silicon layer oxidizes faster where the silicon ions are implanted than where the silicon ions are not implanted, wherein said silicon dioxide has substantially uniform thickness throughout said exposed region, wherein said kinetically regulating silicon oxidation is performed through said opening having a width that is substantially the same at said implanting as it is at said heating and said exposing, and wherein no additional layer is formed within said opening during said kinetically regulating silicon oxidation.

45. (Once Amended) A method as recited in Claim [1] 47, wherein said [bombarding an exposed region is performed with ions] implantation ions are different from [said] ions of said first semiconductor material.

46. (Once Amended) A method as recited in Claim [1] 47, further comprising bombarding through said unmasked region with implantation ions that are [said exposed region of a volume of semiconductor material composed of a first material with ions] different from [said] ions of said first semiconductor material.

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